REMARKS

This is in response to the Office Action dated July 17, 2006. Claims 1-3 and 5-23 are pending.

Claim 1 stands rejected under Section 102(e) as being allegedly anticipated by Yoon. This Section 102(e) rejection is respectfully traversed for at least the following reasons.

In making the rejection, the Office Action contends that M16 and M19N in Fig. 6 of Yoon are transistors which are connected "in series."

In order to further define over Yoon, claim 1 has been amended to require that (1) *the first and second NMOS transistors are directly connected to each other in series* and/or (2) *the first and second PMOS transistors are directly connected to each other in series*. This change to claim 1 is intended to prevent the Examiner from contending that in Fig. 6 of Yoon elements M16 and M19N are the claimed first and second NMOS transistors, and/or from contending that M15 and M19P are the claimed first and second PMOS transistors.

For example and without limitation, figures of the instant application illustrate a cell which includes PMOS section M05 comprising PMOS transistors M05a and M05b connected directly in series, and an NMOS section M06 including NMOS transistors M06a and M06b connected directly in series (e.g., see Figs. 2B, 5B, 10B, 13B-15B, etc.). Thus, the instant specification supports the claim language which requires that (1) *the first and second NMOS transistors are directly connected to each other in series* and/or (2) *the first and second PMOS transistors are directly connected to each other in series*.

Yoon fails to disclose or suggest that (1) *the first and second NMOS transistors are directly connected to each other in series* and/or (2) *the first and second PMOS transistors are directly connected to each other in series*, as required by claim 1. Instead, in Fig. 6 of Yoon, the

PMOS transistor M15 of M16 and the PMOS transistor M19P are *not* connected directly in series; they are not connected directly in series because inverter devices M17, M18 and driver-register circuit 618 are provided therebetween. Moreover, in Fig. 6 of Yoon, NMOS transistors M16 and M19N are not connected directly in series because driver-register circuit 618 is provided therebetween. Moreover, one of ordinary skill in the art would never have removed elements 618, M18 and M18 from Fig. 6 of Yoon.

In view of the above, it is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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